

## Time Loss Through Gating of Asynchronous Logic Signal Pulses

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**Abstract**—The gating of asynchronous signals causes logical errors. It is possible to reduce the frequency of these errors, but the price paid is a severe loss of time and extra cost in hardware.

Consider Fig. 1. Suppose  $B$  is an asynchronous signal entering some clocked logic with clock  $A$ , and it is brought into synchronization by ANDing ( $A.B$ ). There is a statistical possibility that chaos will result, as indicated by the special case in Fig. 1. For example, line  $G$  might indicate that data transfer had taken place at time  $t_1$ ,

although line  $H$  only enabled the transfer to take place at time  $t_2$ .

A first (insufficient) step is to make  $C$  drive a bistable, as in Fig. 2. However, there is still a (smaller) statistical possibility that chaos will result, as indicated by the special case in Fig. 2, because the flip-flop may enter its metastable (half-set) state for an extended period of time. As a result, the system will still get out of step. For discussion of this metastable state, see Appendix I.

The gating of asynchronous signals will always carry a statistical chance of logical failure, because it carries with it the risk of the appearance of a half-amplitude, half-true logic signal. The inter-

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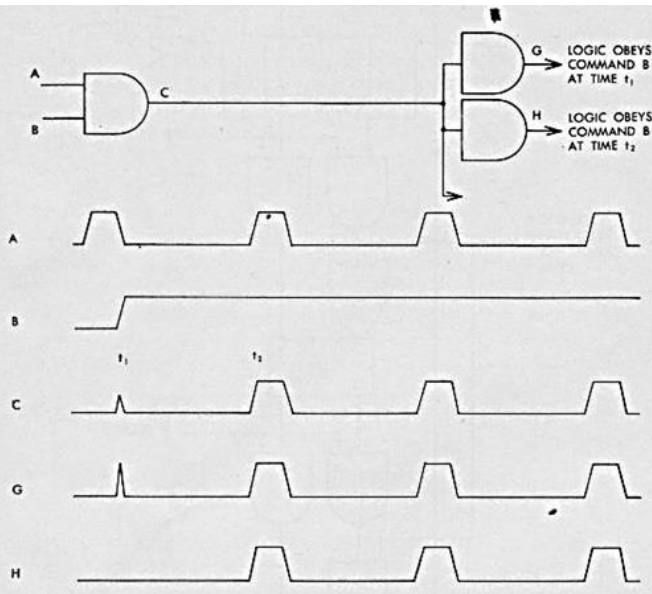


Fig. 1.

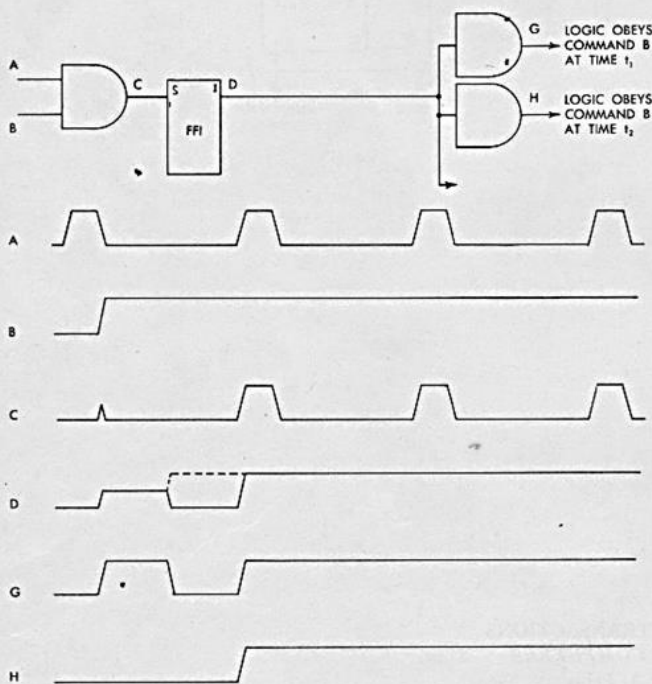


Fig. 2.

mittent failure resulting is more serious than a catastrophic failure, because it introduces undetected errors.

The following is a description of how to reduce the failure rate to acceptable proportions. A good rule of thumb for acceptable failure rate for a logical circuit is one failure in about 1000 days, or three years.

Figure 3 shows the circuit. (*A.B*) tries to set FF1 at time  $t_1$ . At time  $t_2$ , after a delay of length  $t$ , the output of FF1 is interrogated, and it is hoped that FF1 will by that time have left its metastable state and returned to one or other of its stable states, so that during one of the clocks *E*, FF2 will be set unambiguously. The probability that at time  $t_2$ , FF1 will still be metastable and, therefore, that a failure will occur in spite of its protective circuitry, is computed in Appendix II. It is easy to make this probability acceptably low. Unfortunately, the time  $(t_2 - t_1)$  lost in the process is uncomfortably large.

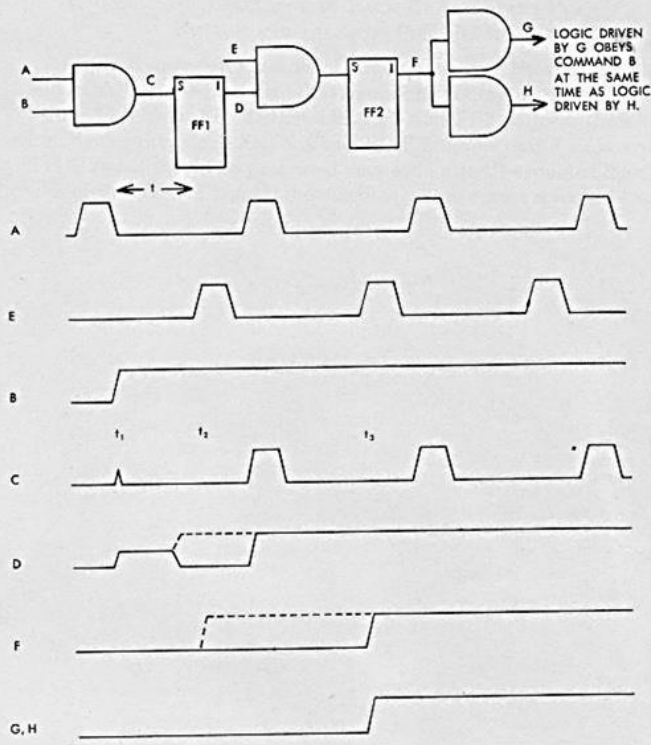


Fig. 3.

#### APPENDIX I

##### DISCUSSION OF THE METASTABLE STATE

Figure 4 shows the transfer characteristics of the two halves of a bistable. The transfer characteristic for the first half is drawn in the first and third quadrants. The transfer characteristic for the second half is drawn in the second and fourth quadrants. The letter *M* shows the metastable state. The bistable can continue indefinitely in this state; this is possible even in a noisy environment. There is a certain pattern of random noise which will alternately move the bistable to one side and the other of its metastable state, but not far enough for it to move to one of its two stable states.

It is possible for the bistable to continue indefinitely in its metastable state if the transfer characteristics of the two halves of the bistable differ. Figure 5 shows the case where the first half of the bistable has a low threshold and the second half has a high threshold. The metastable state is where the two curves intersect.

The dotted line in Fig. 4 shows the case when the spike *C* in Fig. 3 has pushed the bistable near to its metastable state—in this case, slightly further than the metastable state. We can see the events that follow by going clockwise, starting with the first quadrant. In this case the bistable gets out of the transition region in a time  $2d$ , or twice round the loop in the bistable.

The practical case of a metastable state will be more complex than the steady-state picture described previously. In practice, the metastable state might be represented by an oscillation of the bistable outputs about a mean level represented by the steady metastable state. This is the situation investigated in Appendix II.

#### APPENDIX II

##### CALCULATION OF FAILURE RATE

In Fig. 3, let us assume that the number of times per second that *B* goes true (and, therefore, there is a chance of failure) is  $f$ . A reasonable figure for  $f$  when multiplexing data transfers from a number of tape stations into a computer would be  $10^8$ .

If we are considering a three-year period (equals about  $10^8$  seconds), then the number of times *B* goes true is about  $10^8 \times f$ . If

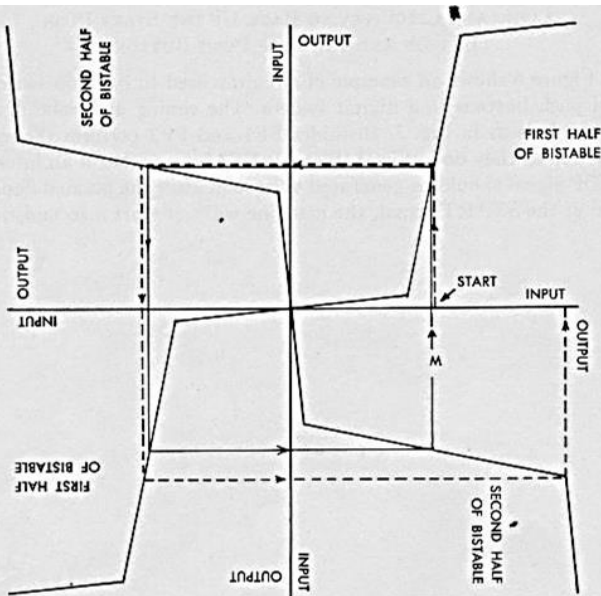


Fig. 4.

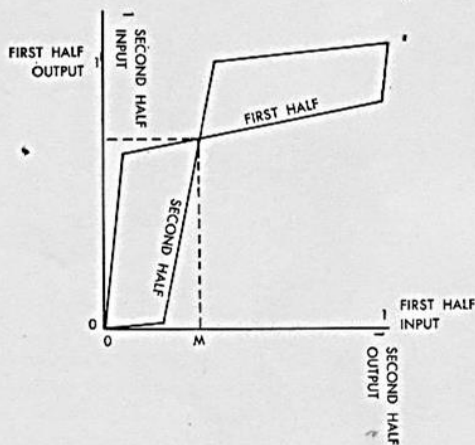


Fig. 5.

we allow one failure during this time, we allow a failure probability of  $1/10^8 \times f$ .

The first bistable is driven into its metastable state if the width of the spike occurring at C at time  $t_1$  is less than the delay around the loop in bistable FF1. If the transistor frequency bandwidth is  $F$ , then the delay around the bistable will be approximately  $10/F$  seconds.

If  $B$  goes positive  $f$  times per second and  $f \ll F$ , then the proportion of times that the trailing edge of  $A$  catches  $B$  and generates a spike is

$$\left[ \frac{10}{F} \right] \left[ \frac{1}{1/f} \right] = \frac{10f}{F}$$

Thus, the number of times in three years when a small spike occurs is

$$10^8 f \times \frac{10f}{F} = \frac{10^9 f^2}{F}$$

Let us assume that

$$R = \frac{\text{Transition region amplitude}}{\text{Logic swing}}$$

Then  $R$  represents the proportion of the small spikes which will be of such amplitude as to partly succeed in setting bistable FF1, and so FF1 enters its metastable state  $(10^9 f^2 \times R)/F$  times in three years.

We now have the picture of a roughly half-sized pulse recirculating around the feedback loop of the bistable FF1. We may assume that there is a regular distribution of amplitudes among these pulses, starting with small ones which just get into the transition region, through pulses nearly half way through the transition region, to large pulses which are only just below the top of the transition region.

Each time this pulse passes around the loop, it is amplified twice. If the amplification in each half of the bistable is  $\beta$ , the amplification around the loop is  $\beta^2$ . In one trip round the loop, a number of pulses will drop out of the transition region. After  $n$  trips round the loop, the number of pulses still within the transition region will decrease by a factor  $(1/\beta)^{2n}$ .

Now we must wait so long that only one pulse remains in the transition region during three years. This means that

$$1 = \frac{10^9 R}{F} \times \left[ \frac{1}{\beta} \right]^{2n}$$

Therefore, the number of times that the pulse must be allowed to circulate round the bistable loop is

$$n = \frac{1}{2} \frac{\log \left[ \frac{10^9 R}{F} \right]}{\log \beta}$$

The time  $t$  in Fig. 3  $= n \times d$  where  $d$  is the delay round the loop of the bistable.

#### Example

As an example, let us substitute the following values into the formula:

Number of times per second that signal  $B$  arrives  $= f = 10^6$

$$\frac{\text{Transition width}}{\text{Signal logic swing}} = R = \frac{1}{10}$$

Frequency bandwidth of the transistors  $= F = 10^9$

Gain of one half of the bistable  $= \beta = 5$

Delay round the bistable  $= d = 10/F = 10$  ns. Then,

$$n = \frac{1}{2} \frac{\log \left[ \frac{10^9 \times 10^6}{10^9} \times \frac{1}{10} \right]}{\log 5} = \frac{1}{2} \times \frac{20.7}{1.61} = 6.4$$

Now  $d = 10$  ns,

$$\therefore t = n \times d = 64 \text{ ns.}$$

#### Worst-case delay

The worst-case (longest) delay will be greater than 64 ns for two reasons:

1) In Fig. 3, the worst-case delay is  $(t_3 - t_1)$ . This equals  $2t$  plus (say) 20 ns. This 20 ns allows for the length of pulses  $E$  and  $A$  and also the gap between them, so thus, we have a delay of  $2t + 20$ .

2) The 64 ns was computed on the basis of various tenuous assumptions. The author considers that for safety, it should be doubled. This gives a total delay of  $4t + 20 = 276$  ns.

Thus, we end up with a worst-case delay of about 300 ns. Note that this is when using transistors with a frequency bandwidth of the order of 1 Gc/s.

### APPENDIX III

#### DISCUSSION OF THE SOLUTION TO THE PROBLEM

Figure 3 shows the circuit and timing diagram which solves the problem as far as it is possible to solve it. What is necessary is to get the logic signals out of the transition region as they enter the system. The basic element of a successful circuit is a very high-gain digital stage. That is, we need an element with a very narrow transition region. This can be achieved by placing a number of logic elements in series. However, it seems easier to use only two logic elements cross coupled. The result is a bistable FF1.

APPENDIX IV

LOGIC AND CIRCUITRY TO BACK UP THE START PUSH BUTTON AND THE STOP PUSH BUTTON

Figure 6 shows an example of circuitry used to back up switches and push buttons in a digital system. The timing of Strobe A and Strobe E is as in Fig. 3. Bistables FF1 and FF2 perform the same function as they do in Fig. 3. Bistable FF3 insures that if an internal STOP signal should be generated very soon after the manual depression of the START signal, the machine will not start a second time.

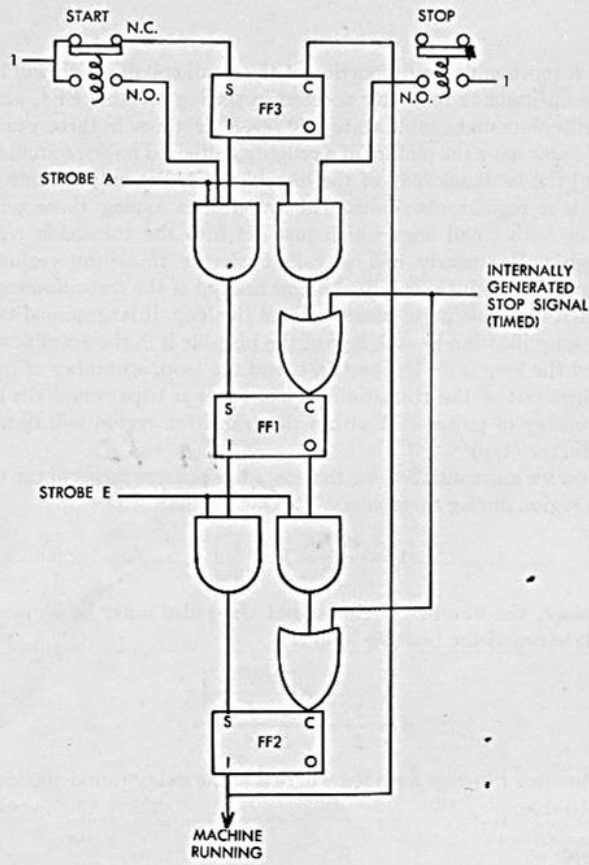


Fig. 6.