# D E A T H  O F
# E L E C T R I C
# C U R R E N T

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articles and
letters

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# PREFACE

Until I write the Definitive Book, this collection of articles and letters from Wireless World will be the best available introduction to the radically new theory of electromagnetism to which I was led as a result of my pioneering work on the interconnection of high speed ( 1 nsec ) logic at Motorola, Phoenix, Arizona, in the early 60's.

If you can afford the delay, I strongly advise you to take some two or three years reading this book. Read just a little bit, then lay it aside for a month or two. Then read a little more, and so on. You will find it very difficult to adjust to the radical change in approach that is needed. Should you jump the gun and turn to the later pages early on, you will surely pay the price in confusion and delay later on. There is no real substitute for gradual adjustment over a long period of time.

CONTENTS

# ADVICE TO READER

This book is published primarily for the benefit of students starting from scratch who want to master Ivor Catt's revolutionary approach to electromagnetic theory, and how it relates to the old theory, called "Classical Electromagnetism". This book will be the best reference for that purpose for a long time. However, it is not ideally organised for that purpose, since for completeness all articles by Catt and his colleagues on e-m, plus all the resulting letters debating the issues raised, have been included. The serious student might prefer to be guided away from these latter letters. The picture is further confused, because whereas some of the Catt articles give a gradually unfolding development of his theories, others serve other purposes - some discussing detailed engineering questions about putting together digital systems, and some attacking classical electromagnetism on its own ground, in its own terms. The student anxious to master Theory C, the new theory of electromagnetism,

should avoid both of these, and study them at another time.

The student anxious to master Catt's revolutionary theory, Theory C, should work through only those articles on pages 34,41,51,86,111,134, plus the letters which arise therefrom. (Had he not refused its re-publication, Bell's article, page 60, would have been one such "letter".) I strongly advise the student, if he can afford the delay, to take a very long time in reading through this series of articles and letters, delaying for two nths each time before tackling the next article in the series, so that his period of very difficult study takes a year or more. However, at any time before, during or after this study period, he can go through the other two sequences of articles as fast as he likes. Articles about practical digital electronic design are on pages 12,23,28,123. Articles attacking classical electromagnetism in its own terms are on pages 73,184,190,197. In both cases, the associated letters should be read as well.

More detailed advice for student of Theory C.

This is the recommended reading plan. Read articles (a) and letters starting on the following pages;
a34, omitting Appendix,38,a41,45, 47,49,
a51,57,(a60),65,66,67,68bis,70,76briefly,
79,80,83,a86,92thrice,93,94,95,97,98,99,
100,101bis,102bis,103bis,106,107,108,
109bis,110,111,a112,116,117,118bis,120,
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## INDEX

This is a cumulative index covering the two volumes ELECTROMAGNETIC THEORY (E), the two volumes DIGITAL ELECTRONIC DESIGN (D), the out of print Macmillan book DIGITAL HARDWARE DESIGN (M), and Wireless World articles (WW)

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The first four books are at **http://www.forrestbishop.4t.com/** .
Then M is at **http://www.ivorcatt.org/digital-hardware-design.htm**
A 2011 index is at **http://www.ivorcatt.co.uk/200.htm**
Further books at **http://www.ivorcatt.co.uk/em.htm** and
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C.A.M.

# P.c.b. layout for high-speed Schottky t.t.l.

Requirements of printed-board design for low inductance and effective decoupling

by **D. Walton**, B.Sc. (Hons), Ph.D.

A great deal has been written on the subject of logic design and quite comprehensive books appear almost monthly. In general, however, the published material neglects an extremely important area and one which probably gives the most trouble to practising engineers. This area, which is dealt with in the present article, is concerned with the layout of logic on printed circuit boards in order to ensure reliable operation. The impetus for writing this article comes from the author's own experience of the lamentable lack of understanding of these basic considerations.

IT SHOULD not be concluded from the preamble that the subject is a difficult one; indeed the mathematics employed in the present paper is extremely elementary. The problems are caused rather by the historical progression from analogue to digital techniques with the consequent carrying out of well-tried analogue practices into the digital environment. Unfortunately, the requirements for digital circuitry are frequently opposite to those needed by the analogue variety and hence there is a need for a complete reconsideration of the requirements.

## Low inductance bussing

To understand the criteria which determine how the supply and GND lines should be distributed to the t.t.l., first take the case of a t.t.l. gate driving its output line from low to high. For the gate to drive the output line high it must pass current into it. The output line must be considered as a transmission line of impedance $Z_0$ if its length exceeds 10cm. In practice, $Z_0$ will be in the region of 100Ω and for a single logic signal changing from low to high the instantaneous output current will be given by $I_0 = 5/100 = 50\text{mA}$. This current must be obtained from the supply rails in a time comparable to the risetime of the signal. If, for Schottky t.t.l., $t_{r(\min)} \simeq 1.5\text{ns}$, then charge must be transferred from the decoupling capacitor to the gate and hence to the output line in this time. Remember that charge is obstructed from flowing into the gate by the inductance, L, of the loop ABCD in Fig. 1. If this is approximately 2cm square with reasonable track width then, using the formula for parallel wires, $L = \ln(a/r)\,\mu_0/4\pi \approx 30\text{nH}$. The e.m.f. dropped across L will then be given by $E = -L\mathrm{d}i/\mathrm{d}t$. Therefore,

$$E = \frac{30\times10^{-9}\times50\times10^{-3}}{1.5\times10^{-9}}$$

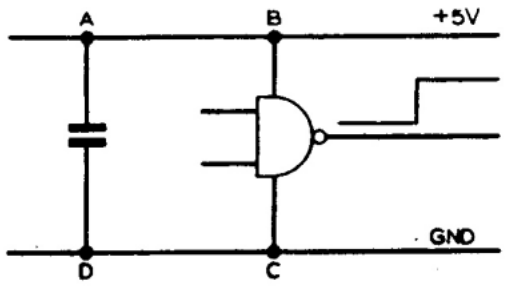


*Fig 1. Example of gate, with decoupling, producing a low-to-high transition.*

$= 1$ volt

This is a considerable voltage and it should be remembered that it is the result of a single gate switching. If all four gates in a pack switch together the currents will be additive and the rail will fall by 4 volts.

The first requirement of a power distribution system must therefore be low inductance between the i.c. and the decoupling capacitor. This is achieved by the track layout shown in Fig. 2(b), where a low inductance path from C to the i.c. is provided by keeping the $V_{CC}$ and GND tracks close together.

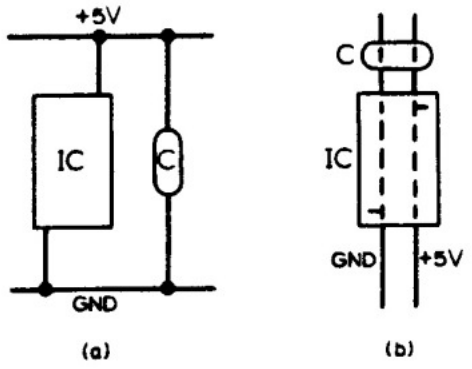


*Fig. 2. Two ways of laying out supply lines. Preferred method, giving lower inductance, is at (b).*

Manufacturers of i.cs usually specify one decoupling capacitor for every 5–10 i.cs which, with the track layout of Fig 2(a) results in prohibitively high inductance between the capacitor and the worst-case positioned i.c. The safest course is to provide the track layout as in Fig. 2(b) but also to put one capacitor adjacent to each i.c. Clearly, this can be achieved by having one capacitor for each pair of i.cs.

## Decoupling capacitors

The foregoing argument shows that the capacitor is better thought of as a reservoir capacitor which supplies the local, instantaneous current demands as i.cs switch. This means that the important parameter for such a capacitor is the instantaneous current which it can supply. Some manufacturers specify capacitors for i.c. decoupling by giving the maximum pulse risetime, which corresponds to a maximum current for a given size of capacitor. For instance, a 47nF capactior specified at 50V/μs can supply a current given by

$$i = C.\frac{dv}{dt} = 47 \times 10^{-9} \times \frac{50}{10^{-6}}$$
$$= 2.5\text{A},$$

which is adequate in the context of the previous calculation.

The other check to make is that the current drawn from the capacitor does not cause its voltage and hence the rail voltage to fall excessively. If the local demand is equal to 10 gates switching, the current demand will be 500mA; to be safe, assume that this demand lasts for 10ns, and design for a voltage drop at the capacitor of 50mV.

Thus,

$$i = C\frac{dv}{dt}$$

$$0.5 = C\frac{50 \times 10^{-3}}{10 \times 10^{-9}}$$

$$C = 100\text{nF}.$$

This suggests that we should provide approximately 100nF for each pair of packages.

It might be thought that radio frequency type capacitors are necessary for t.t.l. decoupling, but this is not so. To show why requires more space than can be spared in an article of this type but essentially it is because the frequently adopted model of a capacitor, which proposes that it possesses a lumped series inductance, breaks down in the case of a single applied step. There is therefore no reason for the designer to be afraid to employ non-ceramic capacitors provided they have adequate V/μs ability. In the author's experience 1μF tantalum beads perform well as decoupling capacitors.

## Transmission-line model

The best way to think of the power distribution system is as a transmission line, with each package connected to an ideal voltage source via an impedance equal to the transmission line impedance*. This impedance must be sufficiently low for negligible voltage transients to be produced on the line by gates switching within the package. The impedance of a transmission line is given by $Z_o = \sqrt{L/C}$, where L and C are the inductance and capacitance per unit length respectively. To calculate $Z_o$ for the case of two tracks close together:

$$L = \frac{\mu_0}{4\pi}\ln\frac{a}{r}$$

where $\mu_r$ is 5. A and r are taken as 2mm and 0.5 mm. Therefore

$$L = 0.6\mu\text{H/m}.$$

If a 100nF capacitor is placed every 5cm along this line, then:

$$C = 100 \times 20\ \text{nF m}^{-1} = 2\mu\text{F m}^{-1}$$

Therefore $Z \approx 0.5\Omega$.

An instantaneous current demand of 200mA – corresponding to 4 gates switching – will produce a voltage transient of 100mV. This is only just acceptable and suggests that the value of C should be increased. Note however, that laying out the tracks with wider spacing and using smaller capacitors – 10nF for every few i.cs, which is not uncommon, will create a situation much worse than this.

## Auto-decoupling in t.t.l.

In the context of the preceding remarks some readers may wonder how systems which they have seen or have worked with managed to function at all, since it is common to see most or all of the above design guidelines violated. To see the answer to this, consider the structure of the t.t.l. gate output circuit, when this is driving the following gate input low, as in Fig. 3.

According to the specification for, say, a 7400 the typical values of i and R are 1.0mA and 4kΩ respectively. When the gate output is low it sinks a current i, given by $i = (V_{cc} - V_{be} - V_{CE(sat)}) / R$, where $V_{be}$ is the base-emitter voltage of $Tr_3$ and $V_{CE(sat)}$ is the collector saturation voltage of $Tr_1$.

If $V_{be}$ and $V_{CE(sat)} = 0.7$ volts, to take a worst-case example, and $V_{cc} = 5$ volts

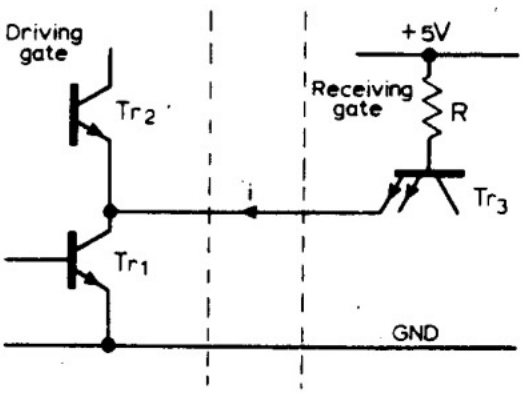


*Fig. 3. Totem-pole t.t.l. output stage, driving succeeding gate low.*

$$\text{then } i = \frac{3.6}{R}$$

Now consider what happens if the rail voltage drops, due to a transient load imposed by the output of another gate switching. When $V_{CC}$ drops there is no change (to a good approximation) in the $V_{be}$ drops. Suppose the rail drops by 10% then:

$$i_1 = \frac{5-1.4}{R}$$

$$i_2 = \frac{4.5-1.4}{R}.$$

Therefore

$$\frac{i_1-i_2}{i_1} = \frac{0.5}{3.6} = 14\%.$$

In other words a 10% change in $V_{CC}$ produces a 14% change in the current load placed on the rail. In effect what is happening is that each gate output which is holding another input low acts as a 'reservoir' of current and when the rail voltage drops as another gate drives its output high all the other gates give up some of their current to assist. This is what I would call the 'good neighbourliness effect' in t.t.l. In general, some gates on a voltage bus will be low and so act as current supplies. The problem arises when none or only a few are in this state – a critical situation for a badly designed system and one which could cause a failure. It should be remembered that a logic system should work for all possible combinations of states which can occur in practice and a hazard of this type could have serious consequences. It is therefore insufficient to demonstrate that a system 'works' because if the power distribution system is badly designed there is always the chance of an untested situation bringing about a failure of the system. It is assumed that in a logic system of reasonable size it is impossible to test all possible combinational situations, and doubly impossible to test all possible changes of situation!

The problem with Schottky t.t.l. is that the increase in speed does not allow time for the 'good neighbourliness effect' to act, consequently one is many times worse off with Schottky than with ordinary t.t.l. Schottky is a less forgiving family than conventional t.t.l. and much more care must therefore be taken with power distribution to ensure reliable performance.

* A package at the centre of a power bus will see two lines in parallel and hence half the impedance. We will adopt the worse figure for the purpose of this argument.

## The current spike

As just described, the main cause of transient current demands in a Schottky t.t.l. system is the initial current surge when a gate switches into its transmission line load. The manufacturers' data overlooks the mechanism entirely. There is another cause of transient current demand which results from the 'push-pull' design of the t.t.l. output stage shown in Fig. 4. The current spike is produced because, on the 0 to 1 transition, the upper transistor turns on while the lower transistor is still turning off. This leads to a current surge of 10mA with duration of about 10ns[1]. Provided the design guidelines laid down in the earlier sections with regard to power supply bussing and decoupling have been followed, this small additional hazard will be taken care of. In fact, since a logic gate is driving a transmission line which is a resistive rather than a capacitive load, there is no need to provide a totem pole output and this must be regarded as one of the bad features of the t.t.l. family.

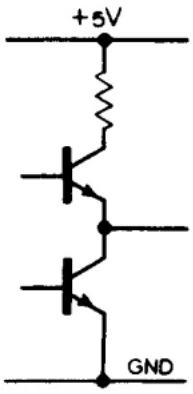


*Fig. 4. T.t.l. output configuration leads to current spike at transmission.*

## Interconnexions

To implement a system successfully using the t.t.l. family it is necessary to interconnect correctly between logic gates.

**Transmission lines.** The correct model to use for interconnexion between logic gates is a two-wire transmission line. It is impossible to understand how a signal travels from gate to gate without taking the return path into consideration. Indeed it is impossible for a signal to travel without a return path! Consider the two-wire transmission line shown in Fig. 5, in which a zero rise-time is propagating to the right with velocity c. Ahead of the step there is no current in the wires and no voltage differences between them. Behind the step there is a current i in the direction of AB and a current -i in the direction of DC with a voltage difference V between the wires. It can be shown[2] that $V = iZ_0$, where $Z_0 = \sqrt{L/C} = \sqrt{\mu/\epsilon}$ where $Z_0$ = characteristic impedance of line, $L$ = inductance per unit length of line, $C$ = capacitance per unit length of line, $\mu$ = permeability of medium between wires, $\epsilon$ permittivity of medium between wires. The velocity of propagation $c = 1/\sqrt{LC} = 1/\sqrt{\mu\epsilon}$.

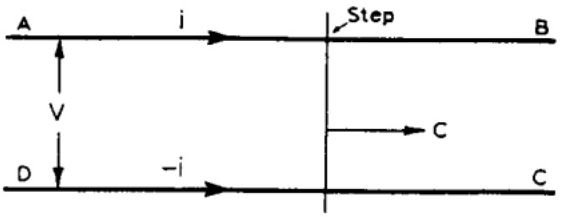


*Fig. 5. Two-wire transmission line.*